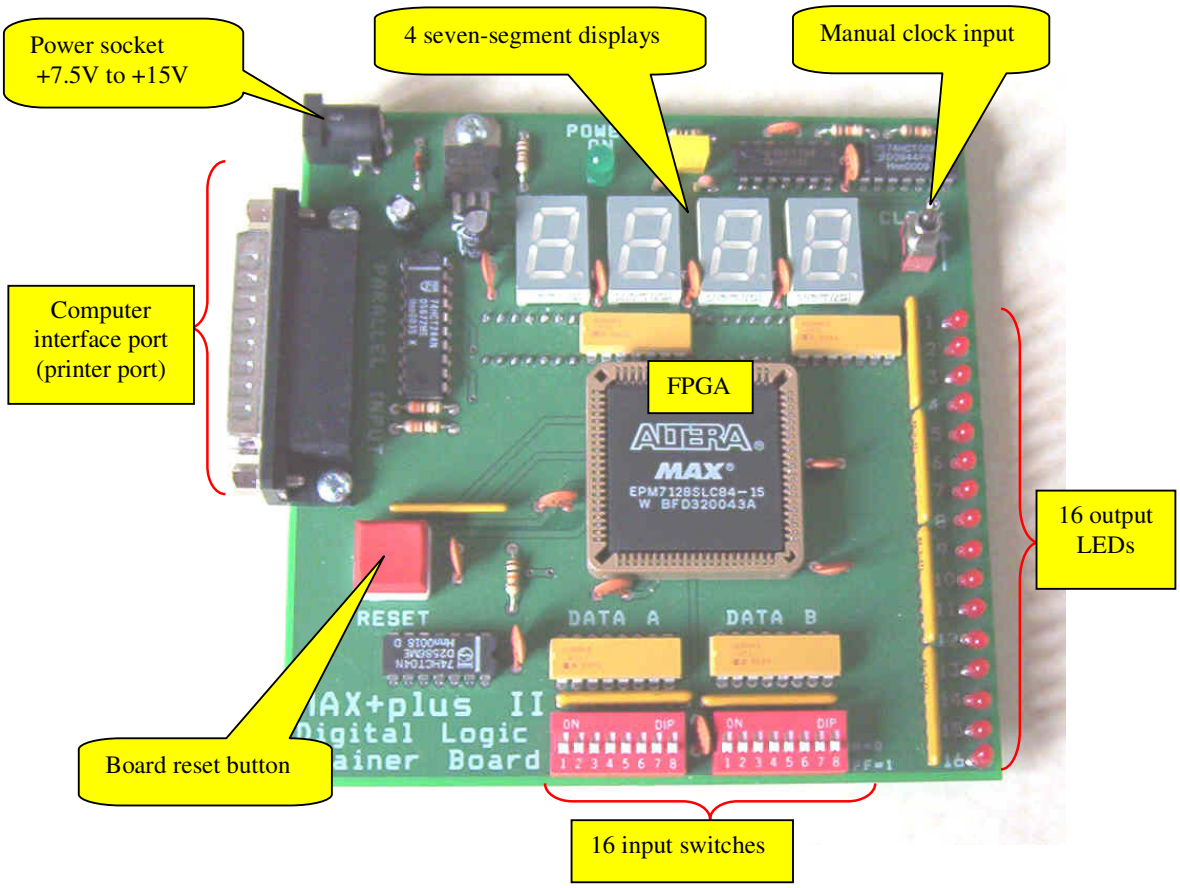
School of Engineering & Physical Sciences
Electrical, Electronic & Computer Engineering

Digital Logic Trainer Board

Board layout



Chip selection

When using the Quartus II development software select the following chip

EPM7128SLC84-15

This chip is a member of the 7000S series.

External connections

Two external connections are necessary to use the board

1.	Power supply in the range 7.5volts to 15 volts. An on-board regulator provides the necessary 5volts. A green LED will be lit when power is correctly applied.
2.	A 25-way male connector is located on the board. This must be connected to your computer printer port to allow designs to be loaded into the board FPGA. The Quartus II development software has a driver to allow it to download designs through this cable.

Device pin assignments

At some point in the design process, you must connect input/output points of your design with the physical pins of the EPM7128SLC84-15. The following is a list of the pin numbers.

Input switches

Data A Switches (1 to 8)	EPM71128SLC84-15 Pin No.
1	22
2	24
3	25
4	27
5	28
6	29
7	30
8	31

Data B Switches (1 to 8)	EPM71128SLC84-15 Pin No.
1	37
2	36
3	35
4	34
5	33
6	39
7	40
8	41

LEDs

LED No.	EPM71128SLC84-15 Pin No.
1	63
2	60
3	61
4	58
5	57
6	56
7	55
8	54
9	52
10	51
11	50
12	49
13	48
14	46
15	45
16	44

7-segment displays

7-seg letter	Pin No for 7-seg 1	Pin No for 7-seg 2	Pin No for 7-seg 3	Pin No for 7-seg 4
a	15	5	75	65
b	12	4	74	64
c	16	6	76	67
b	18	9	79	69
e	20	11	81	73
f	17	8	77	68
g	21	10	80	70

Clock and reset

Pin Name	Pin Number
GClk (500kHz global clock)	83
GClk (manual clock)	2
Reset	1

Refer to the Quartus II quide to learn how to connect to the chip pins.

Board clock

There are two on-board clock sources. A 500kHz source and a manual switch source. These are available through pins 83 and 2 respectively.