Institute of Physics Publishing Journal of Physics: Conference Series **34** (2006) 788–793
doi:10.1088/1742-6596/34/1/130 International MEMS Conference 2006

Variable RF capacitor based on a-Si:H (P-doped) multi-length cantilevers

Y. Q. Fu,[1] S. B. Milne,[1] J. K. Luo,[1] A. J. Flewitt,[1] L. Wang, [1] J. M. Miao, [2] W. I. Milne [1]

[1] Department of Engineering, University of Cambridge, Trumpington Street, Cambridge, CB2, 1PZ, UK

[2] School of Mechanical and Aerospace Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore, 639798

yf229@cam.ac.uk

Abstract. A variable RF capacitor with a-Si:H (doped with phosphine) cantilevers as the top electrode were designed and fabricated. Because the top multi-cantilever electrodes have different lengths, increasing the applied voltage pulled down the cantilever beams sequentially, thus realizing a gradual increase of the capacitance with the applied voltage. A high-k material, H_fO_2, was used as an insulating layer to increase the tuning range of the capacitance. The measured capacitance from the fabricated capacitor was much lower and the pull-in voltage was much higher than those from theoretical analysis because of incomplete contact of the two electrodes, existence of film differential stresses and charge injection effect. Increase of sweeping voltage rate could significantly shift the pull-in voltage to higher values due to the charge injection mechanisms.

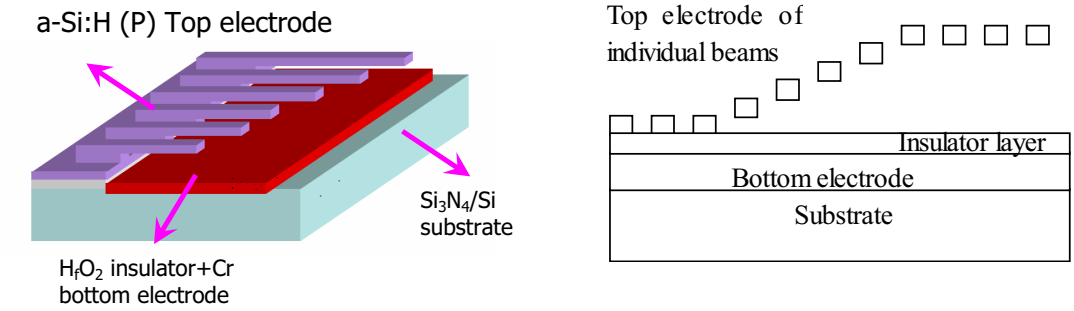
1. Introduction

The application of microelectromechanical systems (MEMS) to radio-frequency (RF)/microwave systems is on the verge of revolutionizing the wireless communications, mainly in the areas of wireless personal communication systems, wireless local area networks, satellite communications, and automotive electronics [1]. RF MEMS enables the superior devices to be made, such as RF switches, tuneable capacitors, inductors and resonators, which are potential for wide usage in home, mobile and satellites. The decrease in size and weight, increased frequency and functionality of the communication systems require the use of highly integrated RF MEMS systems. Among these RF MEMS systems, micromachined tuneable capacitors for RF IC integration are highly demanded. So far, there still exist a lot of problems and shortages associated with the MEMS-variable capacitors. The capacitance values of MEMS-based variable capacitors and tuning range are too small, typically less than a few pF. New designs of the RF variable capacitors and applications of novel materials are necessary. Amorphous and microcrystalline hydrogenated silicon (a-Si:H) thin films have been used in solar cells, thin film transistors in liquid crystal displays, Si based optoelectronics devices and radiation detectors [2]. The a-Si:H film has the potential for the MEMS applications because of its high deposition rate (as high as 100A/s has been reported [3]), relatively low stress, and low deposition temperature (can be as low as 100^{o}C, thus glass and plastics are applicable) [4,5]. The good

electronic properties (with phosphine or boron doped) and reasonable mechanical properties of a-Si:H film suggest that they can be used as the structural layers for thin film MEMS. Although there are some reports on the MEMS applications using a-Si:H film [6-8], they are commonly used as a sacrificial layer for MEMS structure [9]. In this study, a MEMS based variable capacitor were designed and fabricated based on a-Si:H multi-length cantilevers (doped with phosphine) as the top electrodes. A high-k material, H_fO_2, was used as an insulating layer to increase the tuning range of the capacitance. The performance of the fabricated capacitors was evaluated.

2. Design and analysis

The illustration of the designed multi-cantilever variable capacitor is shown in Fig. 1(a). It consists of one bottom electrode (Cr), a top electrode (a-Si:H doped with phosphine) of the suspended multi-length cantilevers overhanging on the bottom electrode, and a layer of high *k* material (H_fO_2) as an insulating layer.



(a) (b)

Figure 1. Illustration of the designed multi-length cantilever based capacitor: (a) layer structure of the capacitor; (b) cross-section illustration of the top beams snapped down with applied voltage

When a bias voltage is applied to the two electrodes in the capacitor, electrical field distribute in such a way that an electrostatic force occurs between them, resulting in pulling of the top electrode towards the bottom one. As the beam moves down, its spring constant changes, creating an opposite mechanical restoring force. When the applied voltage reaches a certain threshold value (or called pull-in voltage, V_{pi}), the mechanical restoring force can no longer balance the electrostatic force, and the cantilever abruptly falls to the bottom contact (see Fig. 1(b)). The pull-in voltage V_{pi} can be calculated using eq. 1 [10].

$$V_{pi} = \sqrt{\frac{8Kd^3}{27\varepsilon_o A}} \qquad 1$$

Where d is the initial gap between the two electrodes. A is the area between the top and bottom electrodes (A=b×L, in which b is the beam width, and L is beam length). ε_o is the permittivity of air. The effective spring constant *K*, can be calculated from eq. 2.

$$K = \frac{Ebh^3}{4L^3} \qquad 2$$

E is the Young's modulus of the a-Si, *h* is thickness of the cantilever. Therefore, the pull-in voltage can be calculated using eq. 1, and the calculated pull-in voltage as a function of the cantilever length with an air gap of 1.5 micron between the two electrodes is shown in Fig. 2. The Young's modulus of the a-Si:H film is chosen as 150 GPa (from the nano-indentation results), and the length of beam is chosen based on the design which is from 60 to 180 μm. The thickness of beam is chosen as 1.2 μm (based on the film deposition results). Results show that the pull-in voltage decreases significantly with the increase in cantilever length.

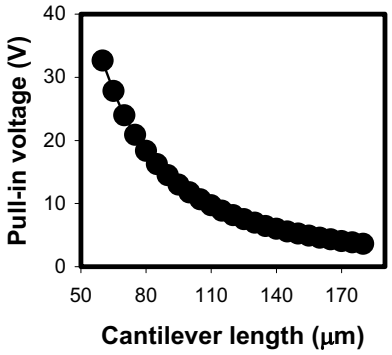


Fig. 2. The calculated pull-in voltage as a function of cantilever length with an air gap of 1.5 μm between two electrodes

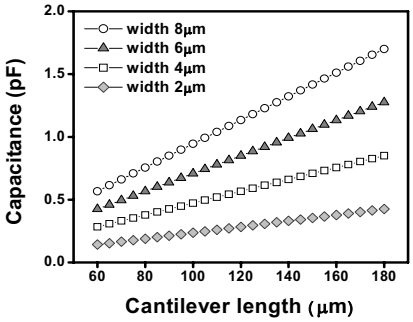


Fig. 3. Calculated capacitance values of the single cantilevers with different lengths and width

For the designed variable capacitor, the top multi-cantilever electrodes have different lengths (or overlapping areas as shown in Fig. 1a). According to Fig. 2, with increase in the applied voltage, the longest cantilever will be firstly pulled down, thus touching the bottom electrode and resulting in an increase in capacitance. With further increase in the applied voltage, the shorter beams will be pulled down sequentially, realizing a discrete increase of the capacitance [11].

A high *k* material, H_fO_2, was used on the top of the bottom electrode to obtain a high isolation and low actuation voltage. It is known that the capacitance C_d can be expressed as:

$$C_d = {A\varepsilon_o k}/{t} \qquad 3$$

Where A is the overlapping area between the top and bottom electrodes. *k* is the dielectric constant of H_fO_2, ε_0 is the permittivity of free-space; t the thickness of the insulating layer. The increase in the capacitance is proportional to the dielectric constant ε of the insulator material. H_fO_2 film has a high dielectric constant, low dielectric loss, low leakage current, high dielectric breakdown voltage, and high isolation ratio [12]. By introducing a layer of H_fO_2, the capacitance value and their tuning range will be increased. The above capacitor has two dielectric materials: (1) the air with a gap d_o and a permittivity of free space ε_0 ; (2) the high-K H_fO_2 insulator with a thickness of t and dielectric constant *k* (*k*=15, from the experimental measurement). Initially, the capacitance of this device is dominated by the dielectric with a low dielectric constant, i.e. the air gap. Whereas it is dominated by the thickness of the insulator when the beams are gradually pulled in. The capacitance, C_i of ith cantilever can be expressed using eq. 4:

$${1}/{C_i} = {1}/{C_{air}} + {1}/{C_{di}} \qquad 4$$

Where C_{air} and C_{di} are the capacitances of the air and the dielectric material (H_fO_2), respectively. Assuming the cantilevers are in full contact with the insulator when pulled-in, the total capacitance of the cantilever beam capacitor, C_t, can be expressed using the sum values of all the cantilevers:

$$C_t = \sum C_i = \sum \frac{C_{di} \times C_{air}}{C_{di} + C_{air}} = \sum \frac{L_i b_i k \varepsilon_o}{d_o \varepsilon_o + tk} \qquad \mathbf{5}$$

Here L_i and b_i are the area, length and width of the *ith* cantilever beam. Fig. 3 shows the calculated capacitance values of the single cantilevers with different lengths and width. The capacitance values increase linearly with increase in both beam length and width. Fig. 4 shows the calculated C-V curves for the designed capacitors with an air gap of 1.5 micron and different beam widths. The capacitance remains a low value initially, but increases significantly after the pull-in of the cantilevers. It continuously increases with the applied voltage due to the pull-down of the shorter cantilever

electrodes. The increase rate gradually decreases because the capacitance value is relatively smaller for the shorter beam lengths.

3. MEMS fabrication process

For the designed variable capacitor, silicon nitride was chosen as the insulating layer on a 4-inch Si wafer. Silicon dioxide was used as the sacrificial layer. Chromium was chosen as the bottom electrode. The top electrode is a-Si:H doped with phosphine. The basic process flow for the MEMS process is schematically illustrated in Fig. 5.

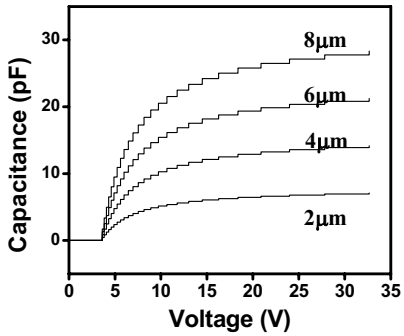


Fig. 4. The calculated capacitance as a function of pull-in voltage

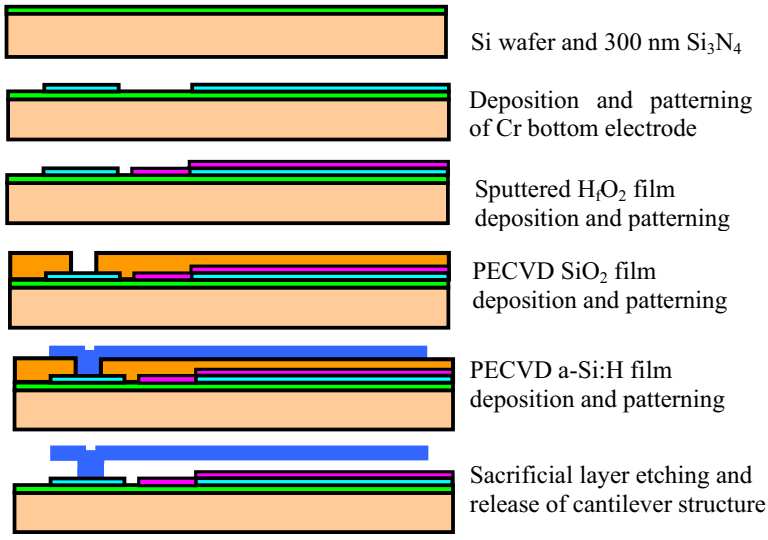


Fig. 5. MEMS process flow of the multi-length cantilever capacitor based on a-Si (P) layer

A 4-inch Si wafer was deposited with a silicon nitride layer of 300nm thick using low-pressure chemical vapour deposition. The bottom electrode of Cr with a thickness of 250 nm was deposited using a magnetron-sputter. The Cr electrode was patterned using Cr etchant. An insulating layer of H_fO_2 with a thickness of 50 nm was sputtering deposited using a lift-off method. A sacrificial layer of SiO_2 of 1.5 micron was deposited at 300^oC using plasma enhanced vapour deposition process (PECVD, radio-frequency 13.56 MHz). The film growth rate is 12nm/min. The SiO_2 sacrificial layer was patterned and etched using the buffered HF wet etchant ($HF:H_2O:NH_4F$=1:6:4) to open the window for a-Si:H film deposition. Phosphorous-doped a-Si:H films of 1.2 micron were deposited at 300^oC using PECVD with a deposition rate of 32 nm/min. To form the top cantilever electrode, the a-Si:H layer was patterned and etched using an reactive ion etching process with SF_6 plasma. The SiO_2

sacrificial layer was then removed using the buffered HF solution etching, thus the free-standing a-Si:H cantilever was released. Stiction is a common problem during the release of a-Si(P) cantilever structure from substrate after wet etching of the sacrificial SiO_2 layer by HF based solution. A freeze dry release method was used in this study to solve this problem. After etching in HF solution, the samples were cleaned in the deionised water, and put into the release agent, Butan-4-ol (with a freezing point of 18^{o}C). The samples were then taken out and the remained release agent was quickly freezed with a cold plate (-5^{o}C) in a chamber. The chamber was then vacuumed to vaporize the solid release agent, and the freestanding cantilever beam structures were successfully released.

4. Characterization and discussion

Figs. 6 show the optical and SEM morphologies of the fabricated RF capacitors. All the cantilevers have been released from the substrate. However, the existence of the differential stress in the a-Si:H films causes the bending of the cantilevers. Optical microscopy observation can show the discrete pull-in phenomana of the multi-cantilevers with the applied voltage. The capacitance measurement as a function of applied voltage was performed using a Boonton capacitance meter. Fig. 7 shows the measured capacitances of the RF capacitor at different sweeping voltage rates. The cantilever beam width is 6 microns. The measured zero-bias capacitance is about 3.7 pF, which is quite large and mainly due to the parasitic capacitance of the thin insulator and low resistivity substrate.

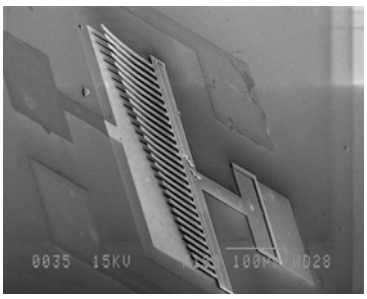


Fig. 6. SEM morphologies of the fabricated capacitors with multi-length cantilevers

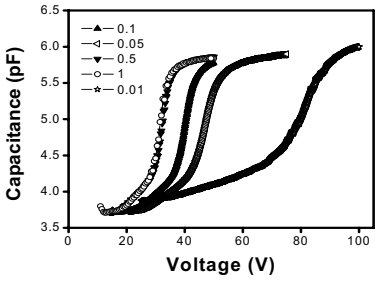


Figure 7. Measured capacitance of the RF capacitor as a function of sweeping voltage rate

Compared with Figs 4 and 7, the measured pull-in voltage is much higher than the calculated values. The calculations from eqs. 1 to 5 are based on the assumption that there is no stress and bending of the cantilevers. The cantilever structures exhibit apparent bending-up due to the stress gradient across the thickness of the beams. It is well known that pull-in voltage is a function of initial curvature of the beam (or the cantilever tip displacement). The larger the initial distance between the cantilever tip and the bottom electrode, the larger the electrostatic force is required to pull-in the structure, which results in an increase in pull-in voltage.

Compared with Figs 4 and 7, the measured capacitance values are also much smaller than the calculated values. Due to the apparent curling-up of the cantilever beams, and large gap between top and bottom electrodes, when the pull-in occurred, the top cantilever beams did not fully contact with the bottom layer (only with an angled contact), which is different from the assumptions in the calculation. Optical microscopy observation showed that after pull-in occurred, each single cantilever was still moved down progressively over the bottom electrode with the increase of voltage. This is the evidence that the contact of two electrodes are an angled contact mode, and could be the main reason that the capacitance values are much smaller than those from the calculated values. Generally it is widely acceptable that the measured capacitance is only about 0.1 times of that calculated value [11,13]. SEM observation (see Fig. 6) clearly showed that there are still some residual sacrificial SiO_2

patterns beneath the top electrodes. The existence of the residual SiO_2 patterns increases the total insulating layer thickness, thus decreases the capacitance values.

From Fig. 7, the sweeping voltage rate has a significant effect on the pull-in voltage. With decrease in voltage rate, the pull-in voltage increases significantly. Both the high K material, H_fO_2, and a-Si(P) are prone to parasitic charging. When the voltage is pulled in, a high electric field across the dielectric builds up causing electrons or holes to be injected into the dielectric and become trapped. With the gradual applied voltage, charge gradually builds up in the dielectric resulting in shift of the pull-in voltage. The amount of charge trapped in the high k H_fO_2 and amorphous Si layer increases with the duration to apply the voltage. The longer the duration, the larger amount of charge trapped in, thus the higher the switch-on voltage, which can explain the voltage rate effect.

5. Conclusions

A variable RF capacitor with a-Si:H (doped with phosphine) cantilevers as the top electrodes were designed and fabricated. Because the top multi-cantilever electrodes have different lengths (or overlapping areas), increasing the applied voltage will pull down the cantilever beams sequentially, thus realizing a discrete increase of the capacitance with the applied voltage. Due to the incomplete contact of the two electrodes, existence of the film differential stresses and charge effect in HfO2 insulating layer and a-Si layer, the measured pull-in voltages are much higher than those from theoretical analysis, whereas the measured capacitance values are much lower.

Acknowledgement

The authors acknowledge the financial support from the European FP6 project PROMENADE (Project No. 507965).

References

[1] H. J. D. L. Santos, G. Fisher, H. A. C. Tilmans, J. T. M. van Beek, IEEE Microwave Mag. 4 (2004) 36-65.
[2] R. W. Collins, A. S. Ferlanto, Current Opinion in Solid State and Mater. Sci., 6 (2000) 425-437.
[3] A. H. Mahan, Y. Xu, D. L. Willaimson, W. Beyer, J. D. Perkins, M. Vanecek, L. M. Gedvilas, B. P. Nelson, J. Appl. Phys., 90 (2001) 5038-5047.
[4] J. P. Conde, J. Gaspar, V. Chu, Thin Solid Films, 427 (2003) 181-186.
[5] Y.Q. Fu, J. K. Luo, S. B. Milne, A. J. Flewitt, W. I. Milne, Mater. Sci. Engng. B, 124 (2005) 132-137.
[6] D. Caputo, G. de Cesare, M. Gavesi, F. Palma, J. Non-Crys. Solids, 338-340 (2004) 725-728.
[7] J. Gaspar, V. Chu, J. P. Conde, J. Appl. Phys., 97 (2005) 094501
[8] J. P. Conde, P. Alpuim, M. Boucinha, J. Gaspar, V. Chu, Thin Solid Films, 395 (2001) 105-111.
[9] C. K. Chung, M. Q. Tsai, P. H. Tsai, C. Lee, J. Micromech. Microeng., 15 (2005) 136.
[10] S. Pamidighantam, R. Puers, K. Baert, H. A. C. Tilmans, J. Micromech. Microeng., 12 (2002) 458-464.
[11] J.K.Luo, M.Lin, Y.Q.Fu, H.Lin, A.J.Flewitt, S.M.Spearing, N.A.Fleck, W.I.Milne, MEMS digital variable capacitors with a high-k dielectric insulator, EUROSENSOR 2005, Sept. 12-15, Barcelona, Spain.
[12] J. Robertson, European Phys. J.-Appl. Phys., 28 (2004) 265-291.
[13] W. M. Van Spengen, R. Puers, R. Mertens, I. De Wolf, J. Micromech. Microeng., 14 (2004) 514-521.